What is claimed is:

1. A flash memory device, comprising:

an array of flash memory cells organized as a plurality of addressable sectors;

control circuitry for controlling operations on the array of flash memory cells; and

a plurality of sector tagging blocks, with each sector tagging block being associated with one sector of memory cells;

wherein each sector tagging block is adapted to generate a select signal having a first logic level when its associated sector is addressed;

wherein the plurality of sector tagging blocks is adapted to generate a common drain signal having a first logic level when any one of the associated sectors is tagged and addressed; and

wherein the plurality of sector tagging blocks is adapted to generate the common drain signal having a second logic level when no addressed associated sector is tagged.

2. The memory device of claim 1, wherein the control circuitry is adapted to erase an addressed sector of the memory device when the common drain signal has its first logic level.

3. The memory device of claim 1, wherein the control circuitry is adapted to scan addresses of the sectors and to erase each addressed sector of the memory device if the common drain signal has its first logic level when that sector is addressed.

4. The memory device of claim 3, wherein the control circuitry is further adapted to scan addresses of the sectors from a first sector address to a last sector address.

5. The memory device of claim 4, wherein the first sector address corresponds to a sector of the memory device other than a first sector of the memory device.

6. A flash memory device, comprising:

an array of flash memory cells organized as a plurality of addressable memory banks, each memory bank comprising a plurality of addressable sectors of memory cells;

control circuitry for controlling operations on the array of flash memory cells, the control circuitry comprising:

a bank decoder having a plurality of outputs, the outputs for respectively providing an output signal corresponding to each bank of the memory device and indicating which bank is selected;

a plurality of inverters, each inverter associated with one of the memory banks and one of the outputs of the bank decoder, each inverter having an input for receiving the output signal from the associated output of the bank decoder and an output for providing a first control signal for the associated memory bank; and

an OR gate having a plurality of inputs, the inputs of the OR gate respectively coupled to the outputs of the bank decoder, an output of the OR gate for outputting a second control signal having a logic high level when any of the outputs of the bank decoder have a logic high level and having a logic low level when all of the outputs of the bank decoder have a logic low level; and

a plurality of sector tagging blocks for each bank, wherein each sector tagging block is associated with one addressable sector of memory cells of a given bank and wherein each sector tagging block comprises:

a sector decoder for receiving a sector address and generating a decoded address signal on an output;

logic circuitry for generating a select signal at an output of the logic circuitry, the logic circuitry having an input for receiving the first control signal from the inverter corresponding to the given bank and an input for receiving the decoded address signal, wherein the select signal is

generated in response to at least the decoded address signal and the first control signal from the inverter corresponding to the given bank;

a first field-effect transistor having a gate coupled to the output of the logic circuitry, a first source/drain region coupled to a third control signal node, and a second source/drain region;

a second field-effect transistor having a gate, a first source/drain region coupled to the second source/drain region of the first field-effect transistor, and a second source/drain region coupled to a first ground potential node;

a latch having an output coupled to the gate of the second field effect transistor and having an input;

a third field-effect transistor having a gate coupled to the output of the OR gate for receiving the second control signal therefrom, a first source/drain region coupled to a supply potential node, and a second source/drain region coupled to the input of the latch;

a fourth field-effect transistor having a gate coupled to a fourth control signal node, a first source/drain region coupled to the input of the latch, and a second source/drain region; and

a fifth field-effect transistor having a gate coupled to the output of the logic circuitry, a first source/drain region coupled to the second source/drain region of the fourth field-effect transistor, and a second source/drain region coupled to a second ground potential node.

7. The memory device of claim 6, wherein the first, second, fourth and fifth field-effect transistors are n-channel field-effect transistors and the third field-effect transistor is a p-channel field-effect transistor.

8. The memory device of claim 6, wherein the latch further comprises a pair of reverse-coupled inverters.

9. The flash memory device of claim 6, wherein the third control signal node is adapted to be pulled up to a supply potential through a pull-up resistor when it is isolated from the first ground potential node.

10. The flash memory device of claim 9, wherein the second control signal node is adapted to be pulled down toward a ground potential when it is coupled to the first ground potential node.

11. A flash memory device, comprising:

an array of flash memory cells organized as a plurality of addressable sectors;

control circuitry for controlling operations on the array of flash memory cells; and

a plurality of sector tagging blocks, wherein each sector tagging block is associated with one sector of memory cells and wherein each sector tagging block comprises:

an address decoder for receiving a sector address on an input and generating a decoded address signal on an output;

a first inverter having an input coupled to the output of the address decoder and having an output;

a first NAND gate having a first input coupled to the output of the first inverter, a second input coupled to a first control signal node, and an output for providing a select signal, wherein the first control signal node is common to each sector of the array of flash memory cells;

a first field-effect transistor having a gate coupled to the output of the first NAND gate, a first source/drain region coupled to a second control signal node, and a second source/drain region;

a second field-effect transistor having a gate, a first source/drain region coupled to the second source/drain region of the first field-effect transistor, and a second source/drain region coupled to a first ground potential node;

a latch having an output coupled to the gate of the second field effect transistor and having an input;

a third field-effect transistor having a gate coupled to a third control signal node, a first source/drain region coupled to a supply potential node, and a second source/drain region coupled to the input of the latch;

a fourth field-effect transistor having a gate coupled to a fourth control signal node, a first source/drain region coupled to the input of the latch, and a second source/drain region;

a fifth field-effect transistor having a gate coupled to the output of the first NAND gate, a first source/drain region coupled to the second source/drain region of the fourth field-effect transistor, and a second source/drain region coupled to a second ground potential node;

a second inverter having an input coupled to a fifth control signal node and having an output;

a second NAND gate having a first input coupled to the output of the second inverter, a second input coupled to the output of the latch, and an output coupled to a third input of the first NAND gate.

12. The flash memory device of claim 11, wherein the array of flash memory cells is further organized as a plurality of addressable memory banks, each memory bank comprising a plurality of addressable sectors, and wherein each memory bank has a first control signal node common to only those sectors contained in that memory bank.

13. The flash memory device of claim 11, wherein the second control signal node is adapted to be pulled up to a supply potential through a pull-up resistor when it is isolated from the first ground potential node.

14. The flash memory device of claim 13, wherein the second control signal node is adapted to be pulled down toward a ground potential when it is coupled to the first ground potential node.

15. A flash memory device, comprising:

an array of flash memory cells organized as a plurality of addressable memory banks, each memory bank comprising a plurality of addressable sectors of memory cells;

control circuitry for controlling operations on the array of flash memory cells, the control circuitry comprising:

a bank decoder having a plurality of outputs, the outputs for respectively providing an output signal corresponding to each bank of the memory device and indicating which bank is selected;

a plurality of first inverters, each first inverter associated with one of the memory banks and one of the outputs of the bank decoder, each first inverter having an input for receiving the output signal from the associated output of the bank decoder and an output for providing a first control signal for the associated memory bank; and

an OR gate having a plurality of inputs, the inputs of the OR gate respectively coupled to the outputs of the bank decoder, an output of the OR gate for outputting a second control signal having a logic high level when any of the outputs of the bank decoder have a logic high level and having a logic low level when all of the outputs of the bank decoder have a logic low level; and

a plurality of sector tagging blocks for each bank, wherein each sector tagging block is associated with one addressable sector of memory cells of a given bank and wherein each sector tagging block comprises:

a sector decoder for receiving a sector address and generating a decoded address signal on an output;

a second inverter having an input coupled to the output of the address decoder and having an output;

a first NAND gate having a first input coupled to the output of the first inverter corresponding to the given bank, a second input coupled to the output of the second inverter, and an output for providing a select signal;

a first field-effect transistor having a gate coupled to the output of the first NAND gate, a first source/drain region coupled to a third control signal node, and a second source/drain region;

a second field-effect transistor having a gate, a first source/drain region coupled to the second source/drain region of the first field-effect transistor, and a second source/drain region coupled to a first ground potential node;

a latch having an output coupled to the gate of the second field effect transistor and having an input;

a third field-effect transistor having a gate coupled to the output of the OR gate for receiving the second control signal therefrom, a first source/drain region coupled to a supply potential node, and a second source/drain region coupled to the input of the latch;

a fourth field-effect transistor having a gate coupled to a fourth control signal node, a first source/drain region coupled to the input of the latch, and a second source/drain region; and

a fifth field-effect transistor having a gate coupled to the output of the first NAND gate, a first source/drain region coupled to the second source/drain region of the fourth field-effect transistor, and a second source/drain region coupled to a second ground potential node.

16. The flash memory device of claim 15, wherein each sector tagging block further comprises:

a third inverter having an input coupled to a fifth control signal node and having an output;

a second NAND gate having a first input coupled to the output of the third inverter, a second input coupled to the output of the latch, and an output coupled to a third input of the first NAND gate.

17. The flash memory device of claim 15, wherein the third control signal node is adapted to be pulled up to a supply potential through a pull-up resistor when it is isolated from the first ground potential node.

18. The flash memory device of claim 17, wherein the third control signal node is adapted to be pulled down toward a ground potential when it is coupled to the first ground potential node.